**MOD N CODE**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_arith.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity mod6 is

Generic (N:integer:=6);

Port ( clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

Q : out integer range 0 to N-1);

end mod6;

architecture Behavioral of mod6 is

signal temp: integer range 0 to N-1;

begin

process (clk,rst)

begin

if clk'event and clk='1' then

if (rst='1' OR temp>=N-1) then

temp <=0;

else

temp<=temp+1;

end if;

end if;

Q <=temp;

end process;

end Behavioral;

**TEST BENCH**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY modntb IS

END modntb;

ARCHITECTURE behavior OF modntb IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT mod6

PORT(

clk : IN std\_logic;

rst : IN std\_logic;

Q : OUT integer range 0 to 5

);

END COMPONENT;

--Inputs

signal clk :std\_logic := '0';

signal rst :std\_logic := '0';

--Outputs

signal Q : integer range 0 to 5;

-- Clock period definitions

constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: mod6 PORT MAP (

clk =>clk,

rst =>rst,

Q => Q

);

-- Clock process definitions

clk\_process :process

begin

clk<= '0';

wait for clk\_period/2;

clk<= '1';

wait for clk\_period/2;

end process;

-- Stimulus process

stim\_proc: process

begin

wait for 100 ns;

rst<='1';

wait for 100 ns;

rst<='0';

wait for clk\_period\*10;

wait;

end process;

END;